32. (New) The integrated circuit of claim 31, wherein the forming source and drain regions further comprises:

providing a pair of spacers abutting lateral sides of the gate structure; and

providing a deep source/drain implant at the source location and the drain location.

33. (New) The integrated circuit of claim 31, wherein the drain extension is formed in a low dosage implant process.

34. (New) The integrated circuit of claim 31, wherein the source extension is formed at an energy level of between 1-5 KeV.

35. (New) The integrated circuit of claim 31, wherein the drain extension is formed at an energy level of between 5-15 KeV.

36. (New) The integrated circuit of claim 31, wherein the first conductivity type is N-type.

37. (New) The integrated circuit of claim 31, wherein the first conductivity type is P-type.

REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow. Claims 1-17 are cancelled without prejudice. Claims 21-37 have been added. No new matter is added.

The Examiner has restricted the Application into two groups, Group I, claims 18-20 and Group II claims 1-17. Applicant has cancelled claims 1-17 without prejudice and hereby elects claims 18-20 and inserts new claims 21-37. New claims 21-37 are drawn to an integrated circuit device.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 5-21-01

By _____

Joseph N. Ziebert
Attorney for Applicant
Registration No. 35,421

FOLEY & LARDNER
Firstar Center
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5367
Telephone: (414) 297-5768
Facsimile: (414) 297-4900

VERSION WITH MARKINGS SHOWING CHANGES

This patent application is related to United States Application Serial No. 09/187,630 (Atty Docket No. 39153-117), filed on 11/6/98 by Yu, titled "Dual Amorphization Implant Process for Ultra-Shallow Drain and Source Extensions" and United States Application Serial No. 09/476,527 [_____] (Atty Docket No. 39153-221) by Yu, on an even date herewith titled "MOS Transistor with Local Channel Compensation Implant." Both applications are assigned to the assignee of the present invention.